

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
13 January 2005 (13.01.2005)

PCT

(10) International Publication Number
WO 2005/003991 A3

(51) International Patent Classification⁷: **G06F 15/78**,
15/80

(21) International Application Number:
PCT/IB2004/051055

(22) International Filing Date: 30 June 2004 (30.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03101975.5 2 July 2003 (02.07.2003) EP

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **PIRES DOS REIS MOREIRA, Orlando, M.** [PT/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **VAN ACHT, Victor, M., G.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **DE OLIVEIRA KASTRUP PEREIRA, Bernardo** [BR/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DE JONG, Durk, J.**; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,

GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

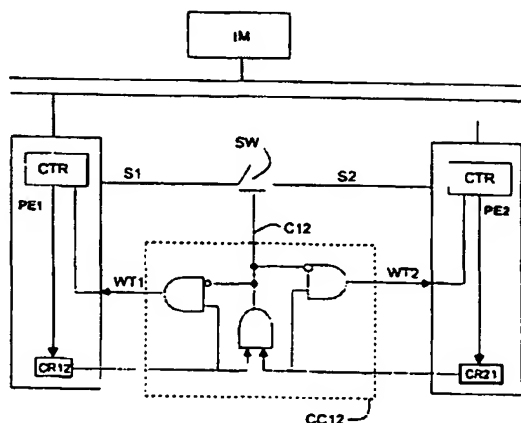
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

[Continued on next page]

(54) Title: SYSTEM, METHOD, PROGRAM, COMPILER AND RECORD CARRIER



(57) Abstract: A processor system is described comprising at least a first and a second processor element (PE1, PE2). The first processor element (PE1) has a cluster request indicator (CR12) related to the second processor element and the second processor element (PE2) has a cluster request indicator (CR21) related to the first processor element. The processor elements have an instruction set enabling dynamic control of the indicators. The indicators (CR12, CR21) have a value range comprising at least a first value (positive indicator) indicating that the processor element requests to form a cluster with the related processor element, and a second value (negative indicator) indicating that the processor element does not request to form a cluster with the related processor element. The system further comprises a cluster control facility (CC12) which detects the value of the cluster request indicator and organizes the processor elements in clusters in accordance

with the detected values. Two processor elements belong to the same cluster if they have positive indicators related to each other, or if there is a sequence of processor elements comprising those two processor elements wherein each pair of subsequent processor elements has positive indicators related to each other.



Published:

- with international search report
- with amended claims

(88) Date of publication of the international search report:
30 June 2005

Date of publication of the amended claims: 1 December 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

AMENDED CLAIMS

[received by the International Bureau on 06 July 2005 (06.07.05);
original claims 1-7 replaced by new claims 1-3 (2 pages)]

1. A processor system comprising at least a first and a second processor element (PE1, PE2), the first processor element (PE1) having a cluster request indicator (CR12) related to the second processor element and the second processor element (PE2) having a cluster request indicator (CR21) related to the first processor element, the processor elements
5 having an instruction set enabling dynamic control of the indicators, the indicators (CR12, CR21) having a value range comprising at least a first value (positive indicator) indicating that the processor element requests to form a cluster with the related processor element, and a second value (negative indicator) indicating that the processor element does not request to form a cluster with the related processor element, the system further comprising a cluster
10 control facility (CCE1, CCE2, ...) which detects the value of the cluster request indicators and organizes the processor elements in clusters, in accordance with the detected values, two processor elements belonging to the same cluster if they have positive indicators related to each other, or if there is a sequence of processor elements comprising those two processor elements, wherein each pair of subsequent processor elements has positive indicators related
15 to each other, the cluster control facility comprising a chain of cluster control elements (CCE1, CCE2, ..) which are coupled to each other via a first wait signal line and a second wait signal line (WSL, WSR), the wait signal lines carrying a signal indicative of whether processor elements coupled to that line should suspend their activities, the cluster control elements being able to modify these signals.
20
2. A processor system according to claim 1, wherein processor elements organized in a cluster operate under a common thread of control.
3. A method for operating a system comprising at least a first and a second
25 processor element, the method comprising programmably controlling a cluster request indicator of the first processor element related to the second processor element and programmably controlling a cluster request indicator of the second processor element related to the first processor element,

the indicator having a value range comprising at least a first value (positive indicator) indicating that the processor element requests to form a cluster with the related processor element, and a second value (negative indicator) indicating that the processor element does not request to form a cluster with the related processor element,

detecting the value of the cluster request indicators and organizing the processor elements in clusters in accordance with the detected values, two processor elements belonging to the same cluster if they have positive indicators related to each other, or if there is a sequence of processor elements comprising those two processor elements, wherein each pair of subsequent processor elements has positive indicators related to each other,

the step of organizing the processor elements in clusters comprising the following substeps,

receiving an input value for a first wait signal and providing an output value for said signal indicating whether the processor receiving said signal is forced to suspend its activities, the output value depending on the input value and a first and a second cluster request indicator,

receiving an output value for a second wait signal and providing an output value for said signal indicating whether the processor receiving said signal is forced to suspend its activities, the output value depending on the input value and the first and the second cluster request indicator.